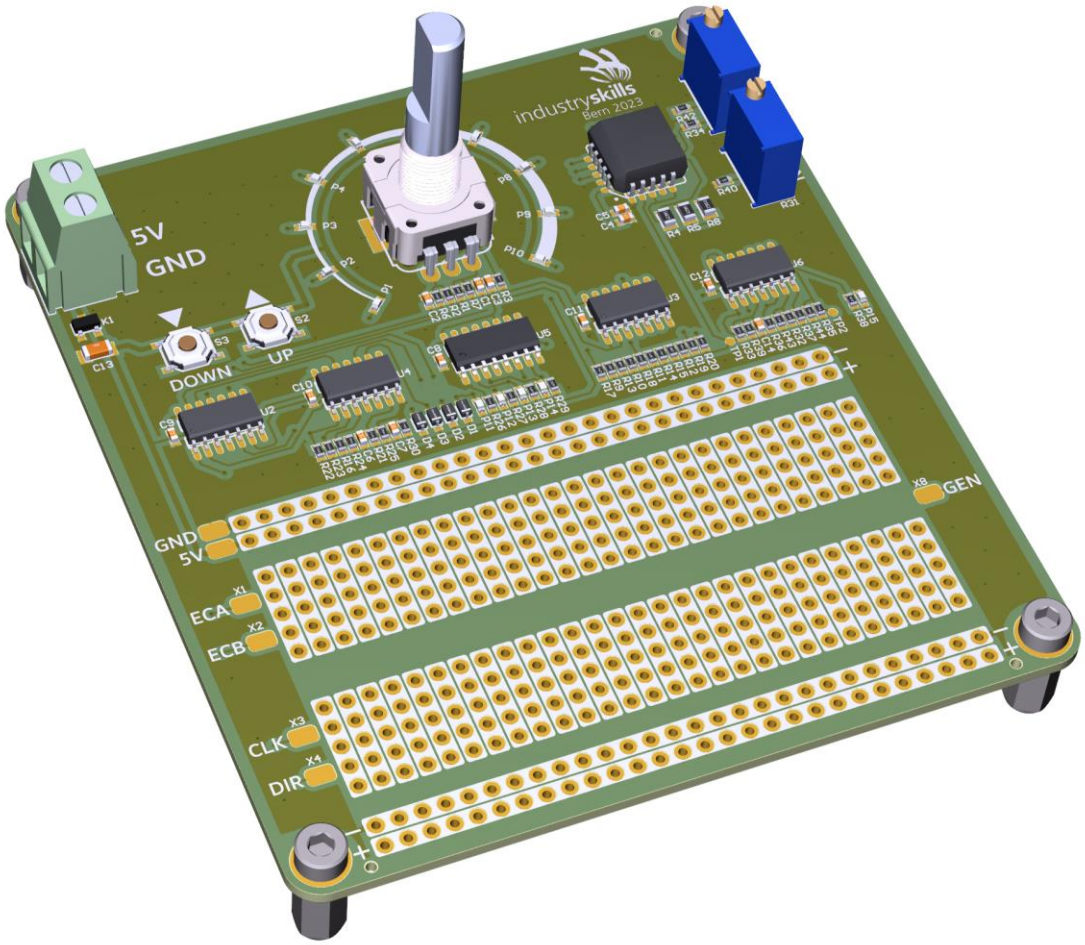
SWISSMEM Berufsbildung

swiss skills Championships | industry skills 2023

Skills: 16 Electronics

Hardware Design

LED-Dimmer with Rotary-Encoder



Hardware Design and Prototyping Task

Table of Contents

1. Contents of this Documentation

This Documentation consists of multiple Documents:

- This task description with Schematic
- PCB (Top-View and Bottom-View)
- BOM (Bill of Material)
- Datasheet LM3914VX
- Datasheet 74HC132D
- Datasheet 74HC74D
- Datasheet MCP6004
- Datasheet NE555P
- Datasheet LTV817
- Datasheet BC547
- Datasheet BC636-16

Please check that you have all of them.

2. Introduction

The provided hardware consists of a rotary encoder that controls the brightness of a LED. In total there are 10 brightness levels (completely off to fully on). The current brightness level is visualized on a LED-Ring around the rotary encoder. In addition to the rotary encoder, the brightness level can also be adjusted with two buttons (labelled “UP” and “DOWN”).
The bottom side of the PCB contains a “bread-board” area where custom circuits can be soldered on. The connections between the holes are identical to commonly used breadboards and are visualized by white bars on the silkscreen.

Time to solve this assignment: 120 min

2.1 Material

Before continuing, please check that you have received the following material:

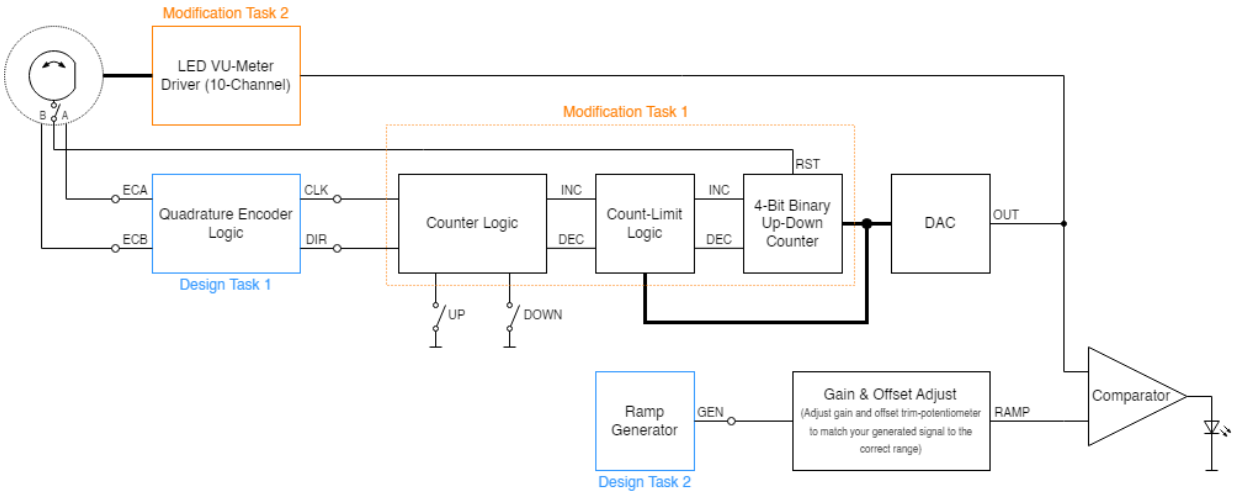
Amount	Components
1 pc	PCB for building your task
1 pc	0805 resistor sample book
10 pcs	100nF 50V SMD capacitor (0805)
3 pcs	1uF 50V SMD capacitor (0805)
3 pcs	10uF 16V SMD capacitor (0805)
4 pcs	1N4148 Diode
3 pcs	BC547 NPN Transistor
3 pcs	BC636-16 PNP Transistor
1 pc	NE555P (Precision Timer)
1 pc	MCP6004 (Rail-To-Rail Input/Output Op-Amp)
1 pc	74HC74D (D-Flip-Flop with Set and Reset)
2 pcs	74HC132D (Quad NAND with Schmitt-Trigger Inputs)
1 pc	LTV817 (General Purpose Optocoupler)

Call an expert in case you are missing any of the above material.

The bag contains all the components required to build the solutions for all 4 Tasks. You will not need all components. Some are superfluous in case you accidentally break some.
Please be careful: If you need to request additional components because you broke all of yours, you will be deducted points!

3. Tasks

In total there are four tasks: Two circuit design tasks and two modification tasks. **You may choose the order in which you design / build these tasks freely.**
The block diagram shows where each task is located, study it carefully.



In the circuit design tasks, points will be awarded both for your designs (functionality and quality) as well as working builds (only functionality) according to the table below:

Circuit Design Task	**Design Points**	**Build Points**
Task 1 (Quadrature Encoder)	10	10
Task 2 (Ramp Generator)	10	20

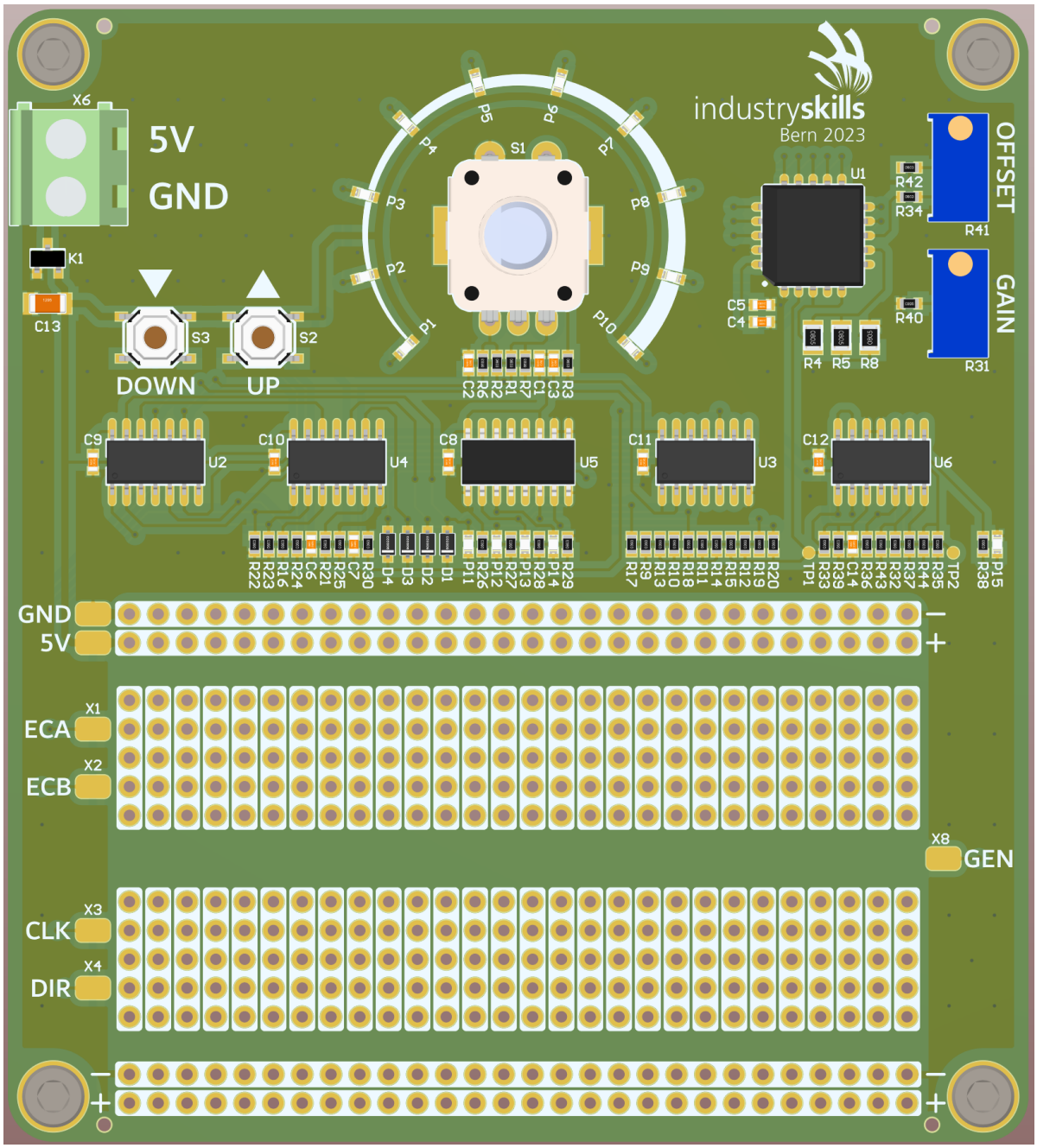
The circuit is not fully working as intended. Find the two faults and correct them. Points will be awarded both for your design modifications (functionality and quality) as well as physical realization (only functionality) according to the table below:

Modification Task	**Design Points**	**Build Points**
Task 1 (Binary Counter)	5	10
Task 2 (LED VU-Meter)	5	5

Draw your designs on the provided sheets in this document below. The design points will be graded by the experts after the assignment finishes.

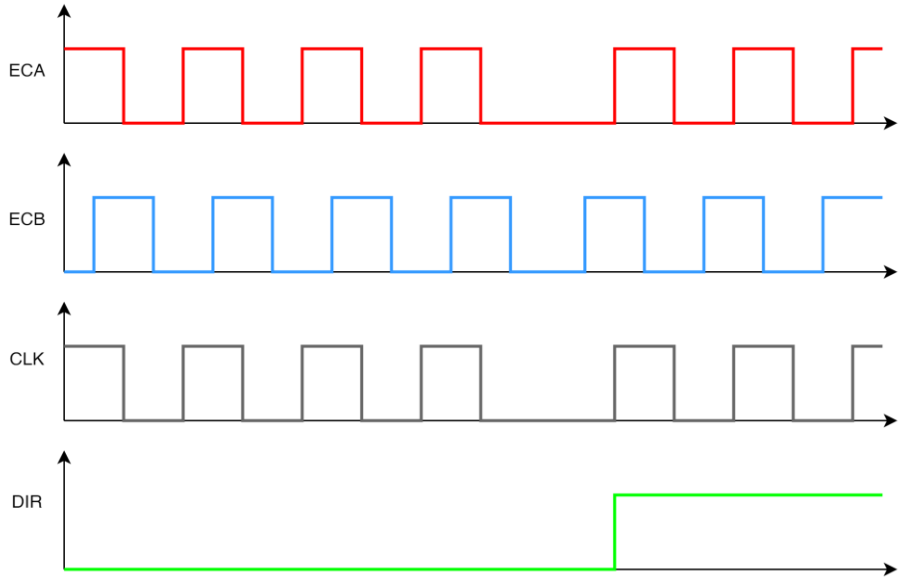
You can use this PCB visualization as a design help to sketch your components and connections. This is **optional** and not part of a task (no points are conducted for this sheet).

Connect your designed circuits to the labelled pads on the side of the prototyping area.



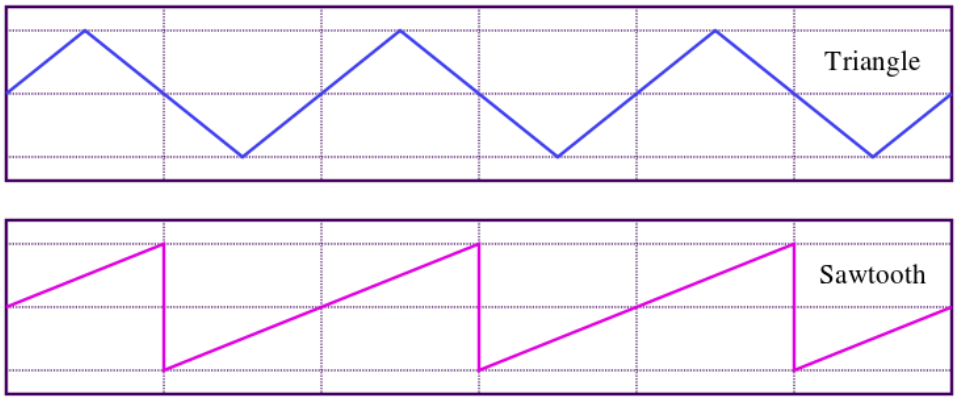
3.1 Design Task 1 (Quadrature Encoder)

Design and build a quadrature encoder logic that converts the rotary encoder signals (ECA & ECB) to a separate clock (CLK) and direction (DIR) signal. Whenever the rotary encoder is turned (both directions) the clock signal should generate a pulse. The direction signal indicates the last measured turning direction (Clockwise → DIR = HIGH, Counter-Clockwise → DIR = LOW).



3.2 Design Task 2 (Ramp Generator)

Design and build a triangle **or** sawtooth generator with a frequency of 500 Hz (± 20%).
You can choose which of the two wave forms you want to generate.
The Amplitude must be in the range of 1.0 … 4.5 Vpp.



Adjust the trim potentiometers (GAIN & OFFSET) so that a PWM signal from 0 to 100% duty cycle can be generated at the output of U6C by adjusting the binary counter between 0 and 10.

3.3 Modification Task 1 (Binary Counter)

The binary counter is not fully counting to 10. Find the fault and correct it.
Note the changes you have made on the solution sheet.

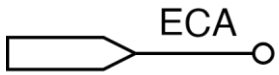
3.4 Modification Task 2 (LED VU-Meter)

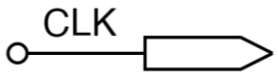
The LED-Ring is not working properly. Modify the VU-Meter circuit, such that for each binary output value, one LED is lighting up (Binary `0000` → no LED is on, Binary `1010` → all LEDs are on).
Note the changes you have made on the solution sheet.

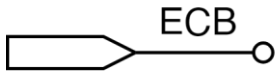
Hint: Make sure you have solved the Modification Task 1 first, since the binary counter must be able to count to 10.

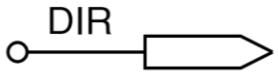
Your solution for Design Task 1 (Quadrature Encoder)

Candidate Name: _____

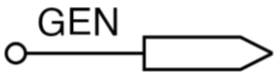






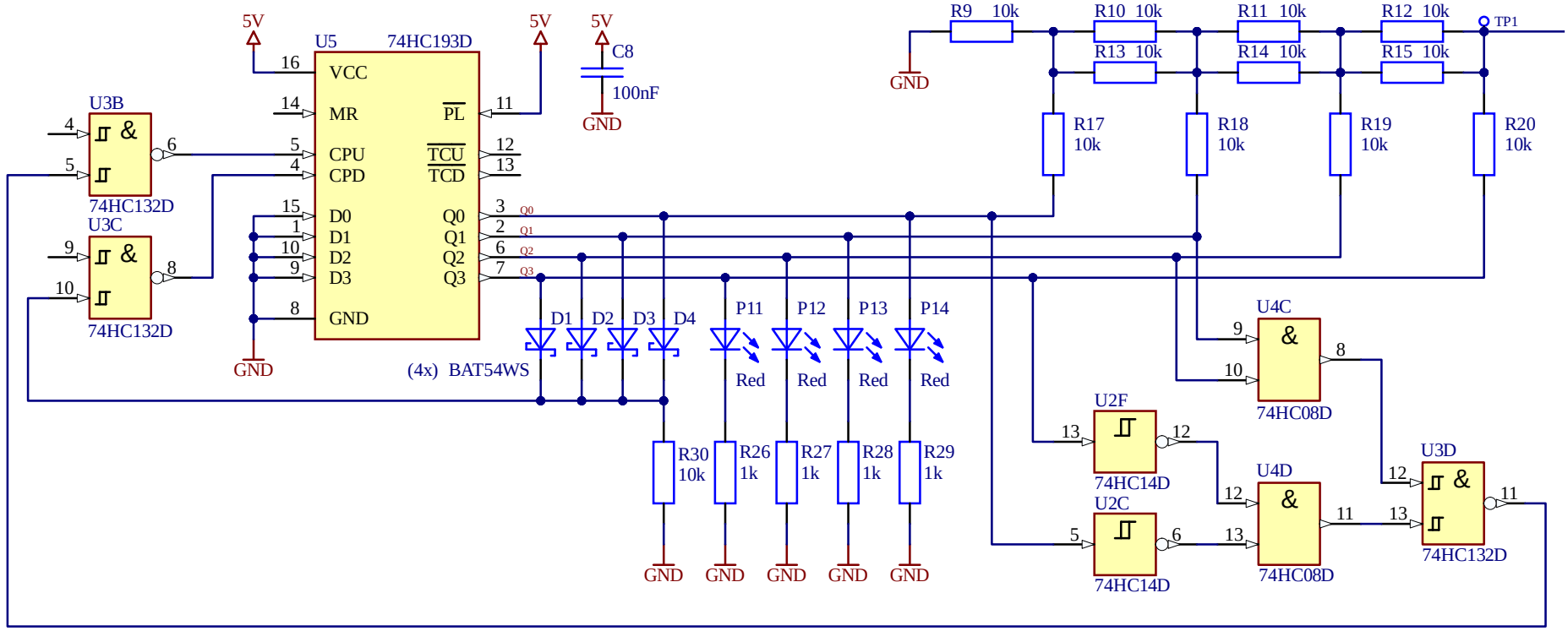


Your solution for Design Task 2 (Ramp Generator)
Candidate Name: _____



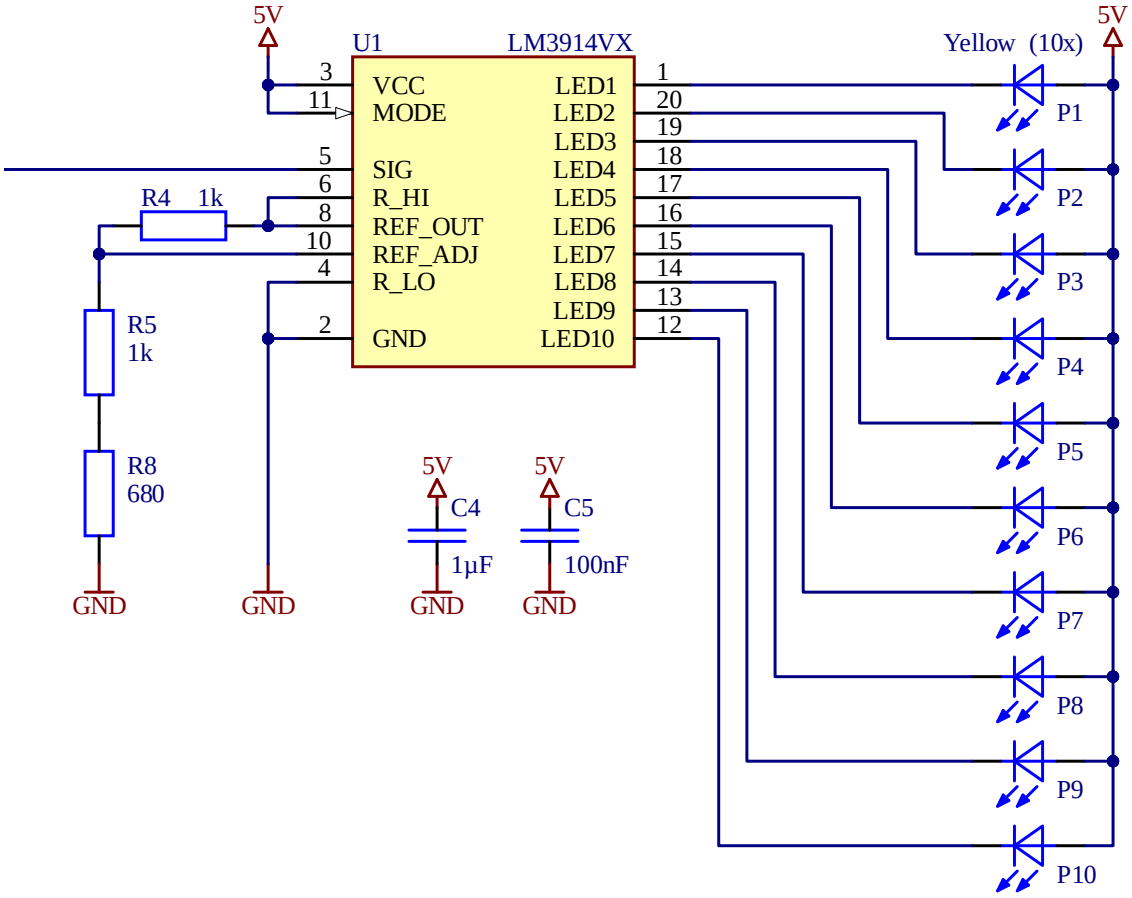
Your solution for Modification Task 1 (Binary Counter)

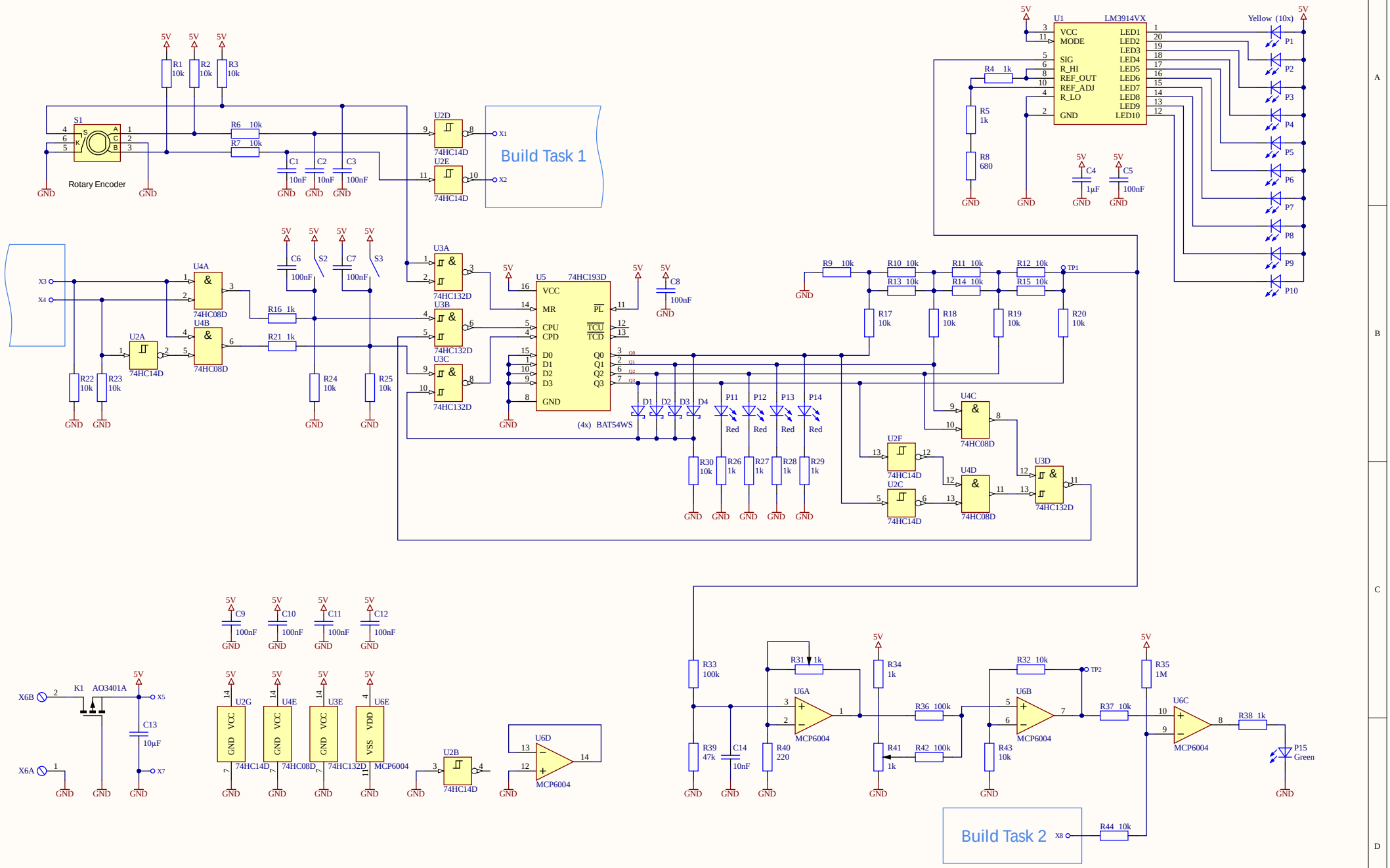
Candidate Name: _____



Your solution for Modification Task 2 (LED VU-Meter)

Candidate Name: _____





Title	**Qualification HW-Design**		
Subtitle	**IndustrySkills 2023 Bern**		
Author: Florian Baumgartner	Date: 18.05.2023	Rev: **V1.1**	
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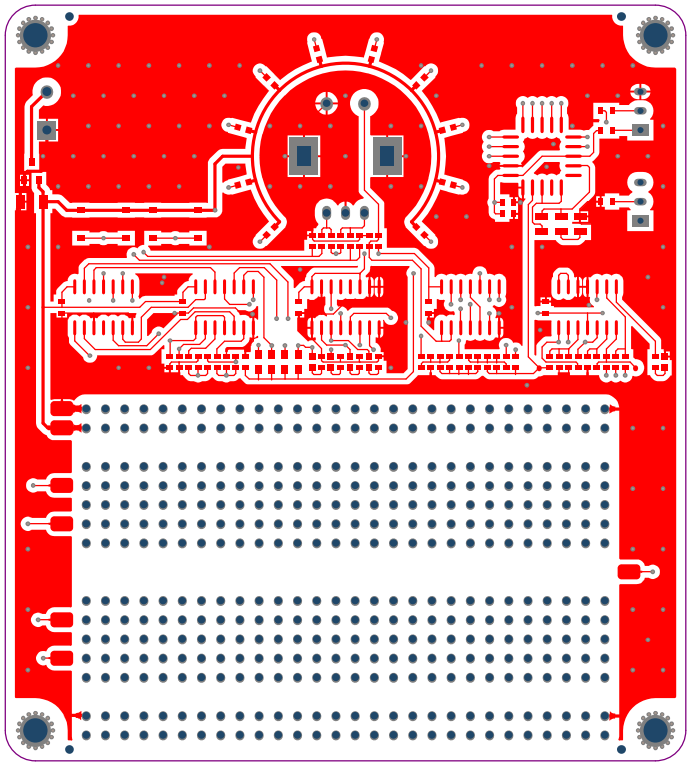

ENGINEER: Florian Baumgartner	TITLE: IndustrySkills 2023 Qualification	
PCB DESIGNER: Florian Baumgartner		
DATE: 03.05.2023	PART NO.: 1/1	REV: V1.0
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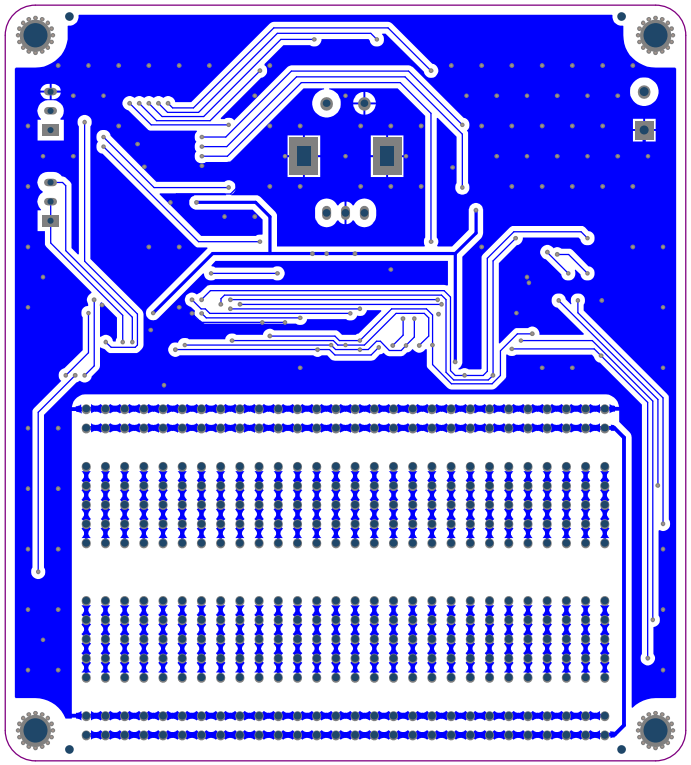

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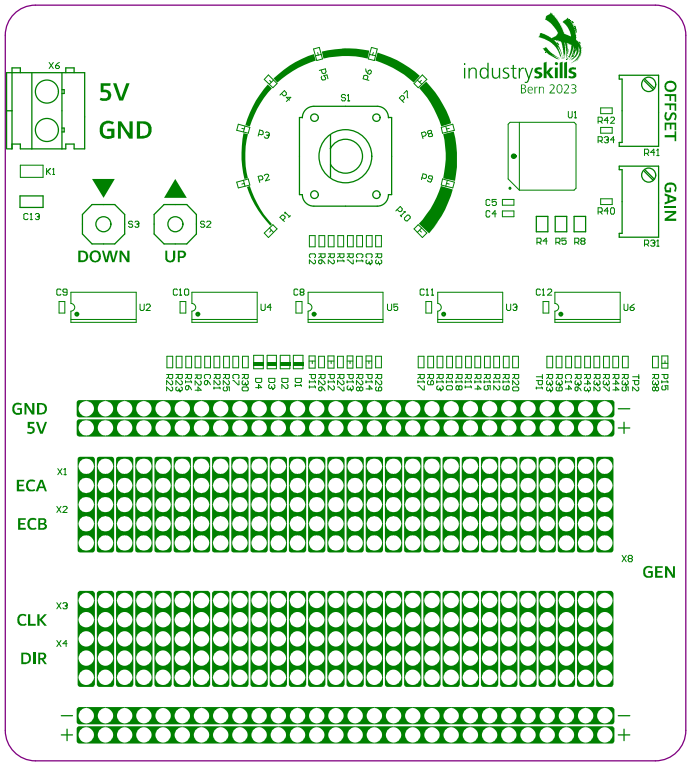

ENGINEER: Florian Baumgartner	TITLE: IndustrySkills 2023 Qualification	
PCB DESIGNER: Florian Baumgartner		
DATE: 03.05.2023	PART NO.: 1/1	REV: V1.0
FILE NAME: IndustrySkills_2023_Qualification_V1.0.PcbDoc	DWG NO: 1/1	SCALE: 1:1

Bill of Materials

IndustrySkills 2023 Qualification

File name: IndustrySkills_2023_Qualification.PrjPcb
Project: IndustrySkills 2023 Qualification
Variant: V1.1

Creation Date: 20.06.2023
Print Date: 20.06.2023

Designator	Component Description	Component Value	Footprint	JLC-Parts	Farnell	Mouser	Digikey	Quantity	Unit Price	Total Price
C1, C2, C14	Multilayer Ceramic Capacitors	10nF 50V	SMD Keramikkondensator 0603	C57112	2346966	77-VJ0603V103ZXAPBC	445-5662-1-ND	3	SFr. 0.01	SFr. 0.03
C3, C5, C6, C7, C8, C9, C10, C11, C12	Multilayer Ceramic Capacitors MLCC	100nF 50V	SMD Keramikkondensator 0603	C14663	2210822	810-CGA2B3X7R1H104K	445-6899-1-ND	9	SFr. 0.01	SFr. 0.09
C4	Multilayer Ceramic Capacitors	1µF 50V	SMD Keramikkondensator 0603	C15849	3013383	187-CL10A105KB8NNNC	1276-1860-1-ND	1	SFr. 0.01	SFr. 0.01
C13	Multilayer Ceramic Capacitors MLCC	10µF 50V	SMD Keramikkondensator 1206	C13585	2113070	963-LMK107BBJ106MALT	587-3258-1-ND	1	SFr. 0.01	SFr. 0.01
D1, D2, D3, D4	Low Voltage Schottky-Diode	BAT54WS-TP	SMD Diode SOD-323	C668868	1924300	833-BAT54WS-TP	BAT54WS-TPCT-ND	4	SFr. 0.20	SFr. 0.80
K1	MOSFET P-Channel	AO3401A	SMD MOSFET SOT-23	C15127			785-1001-1-ND	1	SFr. 0.14	SFr. 0.14
P1, P2, P3, P4, P5, P6, P7, P8, P9, P10	General Purpose LED	Yellow (5mA, 2.0V)	SMD LED 0603	C72038	1465989	645-598-8040-107F	350-2032-1-ND	10	SFr. 0.34	SFr. 3.40
P11, P12, P13, P14	Low Power LED	Red (5mA, 2.0V)	SMD LED 0603	C2286	1465988	645-598-8010-107F	350-2029-1-ND	4	SFr. 0.34	SFr. 1.36
P15	General Purpose LED	Green (5mA, 2.4V)	SMD LED 0603	C72043	1465991	645-598-8070-107F	350-2035-1-ND	1	SFr. 0.34	SFr. 0.34
R1, R2, R3, R6, R7, R9, R10, R11, R12, R13, R14, R15, R17, R18, R19, R20, R22, R23, R24, R25, R30, R32, R37, R43, R44	Thick Film Chip Resistor	10k (75V, 100mW, 1%)	SMD Widerstand 0603	C25804	2303192	667-ERJ-3EKF1002V	P10.0KHCT-ND	25	SFr. 0.01	SFr. 0.25
R4, R5	Dickschicht Chipwiderstand	1k (150V, 125mW, 1%)	SMD Widerstand 0805	C17513	2303550	667-ERJ-6ENF1001V	P1.00KCCT-ND	2	SFr. 0.01	SFr. 0.02
R8	Dickschicht Chipwiderstand	680 (150V, 125mW, 1%)	SMD Widerstand 0805	C17798	2303534	667-ERJ-6ENF6800V	P680CCT-ND	1	SFr. 0.01	SFr. 0.01
R16, R21, R26, R27, R28, R29, R34, R38	Dickschicht Chipwiderstand	1k (75V, 100mW, 1%)	SMD Widerstand 0603	C21190	2303145	667-ERJ-3EKF1001V	P1.00KHCT-ND	8	SFr. 0.01	SFr. 0.08
R31, R41	Trim-Potentiometer	1k (25 Turns)	THT Trim-Poti	C57089	9353178	652-3296W-1-102	3296W-102-ND	2	SFr. 0.19	SFr. 0.38
R33, R36, R42	Thick Film Chip Resistor	100k (75V, 100mW, 1%)	SMD Widerstand 0603	C25803	2303232	667-ERJ-3EKF1003V	P100KHCT-ND	3	SFr. 0.01	SFr. 0.03
R35	Thick Film Chip Resistor	1M (75V, 100mW, 1%)	SMD Widerstand 0603	C105578	2303325	667-ERJ-3EKF1004V	ERJ-3EKF1004V	1	SFr. 0.01	SFr. 0.01
R39	Thick Film Chip Resistor	47k (75V, 100mW, 1%)	SMD Widerstand 0603	C115419	2303213	667-ERJ-3EKF4702V	P47.0KHCT-ND	1	SFr. 0.01	SFr. 0.01
R40	Thick Film Chip Resistor	220 (75V, 100mW, 1%)	SMD Widerstand 0603	C22962	2303090	667-ERJ-3EKF2200V	P220HCT-ND	1	SFr. 0.06	SFr. 0.06
S1	Rotary Encoder with Switch	PEC11R-4025F-S0024	THT Rotary Encoder with Switch	C143799	4014824	652-PEC11L4115FS0020	PEC11L-4115F-S0020-ND	1	SFr. 2.68	SFr. 2.68
S2, S3	Tactile Switch	TS-1187A-B-A-B	SMD Button 5.2x5.2	C318884	3780596	611-PTS526SK15SMR2L	CKN12221-1-ND	2	SFr. 0.02	SFr. 0.04
U1	Dot/Bar Display Driver	LM3914VX	SMD IC PLCC-20	C1519161		926-LM3914VX/NOPB	LM3914VX/NOPBCT-ND	1	SFr. 3.60	SFr. 3.60
U2	Hex inverting Schmitt trigger	74HC193D	SMD IC SOIC-14	C5605	1201316	771-74HC14D-T	1727-2783-1-ND	1	SFr. 0.40	SFr. 0.40
U3	Quad 2-input NAND Schmitt trigger	74HC132D	SMD IC SOIC-14	C5601	1201319	771-74HC132D-T	1727-2780-1-ND	1	SFr. 0.45	SFr. 0.45
U4	Quad 2-input AND gate	74HC08D	SMD IC SOIC-14	C5593	1201314	771-74HC08D-T	1727-2777-1-ND	1	SFr. 0.43	SFr. 0.43
U5	Synchronous 4-bit binary up/down counter	74HC193D	SMD IC SOIC-16	C80043	3119813	771-74HC193D-T	1727-5947-1-ND	1	SFr. 0.82	SFr. 0.82
U6	Low-Power Rail-To-Rail OpAmp	MCP6004	SMD IC SOIC-14	C5342420	1605572	579-MCP6004-I/SL	MCP6004-I/SL	1	SFr. 0.48	SFr. 0.48
X6	Screw-Terminal	WJ500V-5.08-2P (2-Pol, 250V, 8A, 5.08mm)	THT Schraubklemme 2-Pol (WJ500V-5.08-2P)	C8465				1	SFr. 0.08	SFr. 0.08
										SFr. 16.01

Autor

Florian Baumgartner

SWISSMEM Berufsbildung

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LM3914 Dot/Bar Display Driver

Check for Samples: LM3914

FEATURES

- **Drives LEDs, LCDs or Vacuum Fluorescents**
- **Bar or Dot Display Mode Externally Selectable by User**
- **Expandable to Displays of 100 Steps**
- **Internal Voltage Reference from 1.2V to 12V**
- **Operates with Single Supply of Less than 3V**
- **Inputs Operate Down to Ground**
- **Output Current Programmable from 2 mA to 30 mA**
- **No Multiplex Switching or Interaction Between Outputs**
- **Input Withstands ±35V without Damage or False Outputs**
- **LED Driver Outputs are Current Regulated, Open-collectors**
- **Outputs can Interface with TTL or CMOS Logic**
- **The Internal 10-step Divider is Floating and can be Referenced to a Wide Range of Voltages**

DESCRIPTION

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

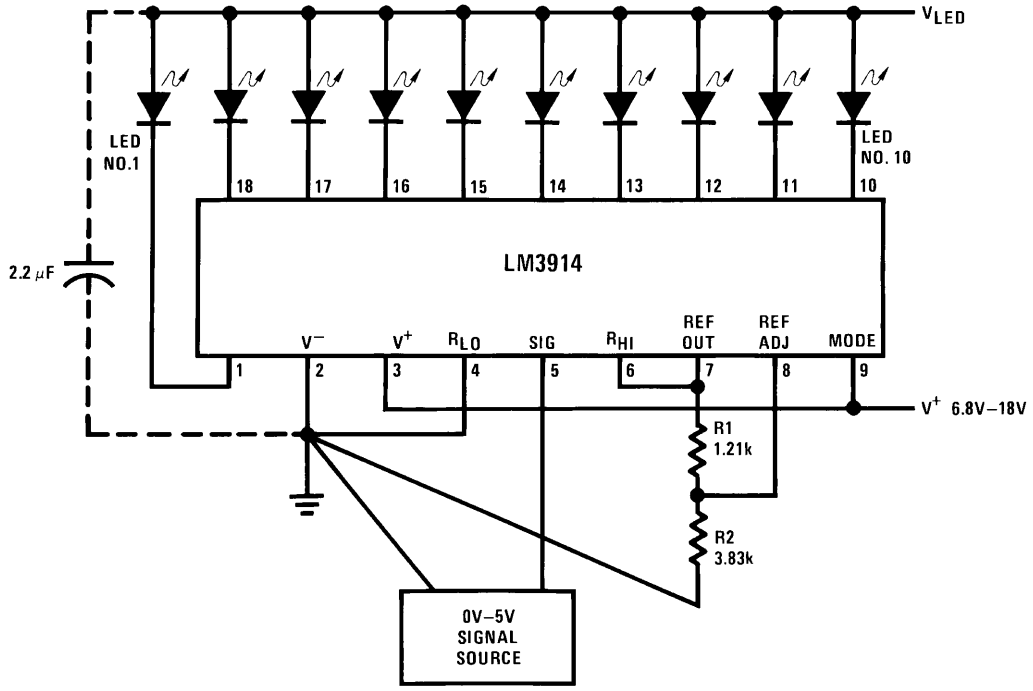
When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N-1 is available in an 18-lead PDIP (NFK) package.

The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

TYPICAL APPLICATIONS



$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \cong \frac{12.5}{R1}$$

Note: Grounding method is typical of *all* uses. The 2.2µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6″ or longer.

Figure 1. 0V to 5V Bar Graph Meter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Power Dissipation (3) PDIP (NFK)	 1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (4)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Soldering Information PDIP Package Soldering (10 seconds)	 260°C
PLCC Package Vapor Phase (60 seconds)	 215°C
Infrared (15 seconds)	220°C
See http://www.ti.com for other methods of soldering surface mount devices.	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the PDIP (NFK package).
(4) Pin 5 input current must be limited to ±3mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

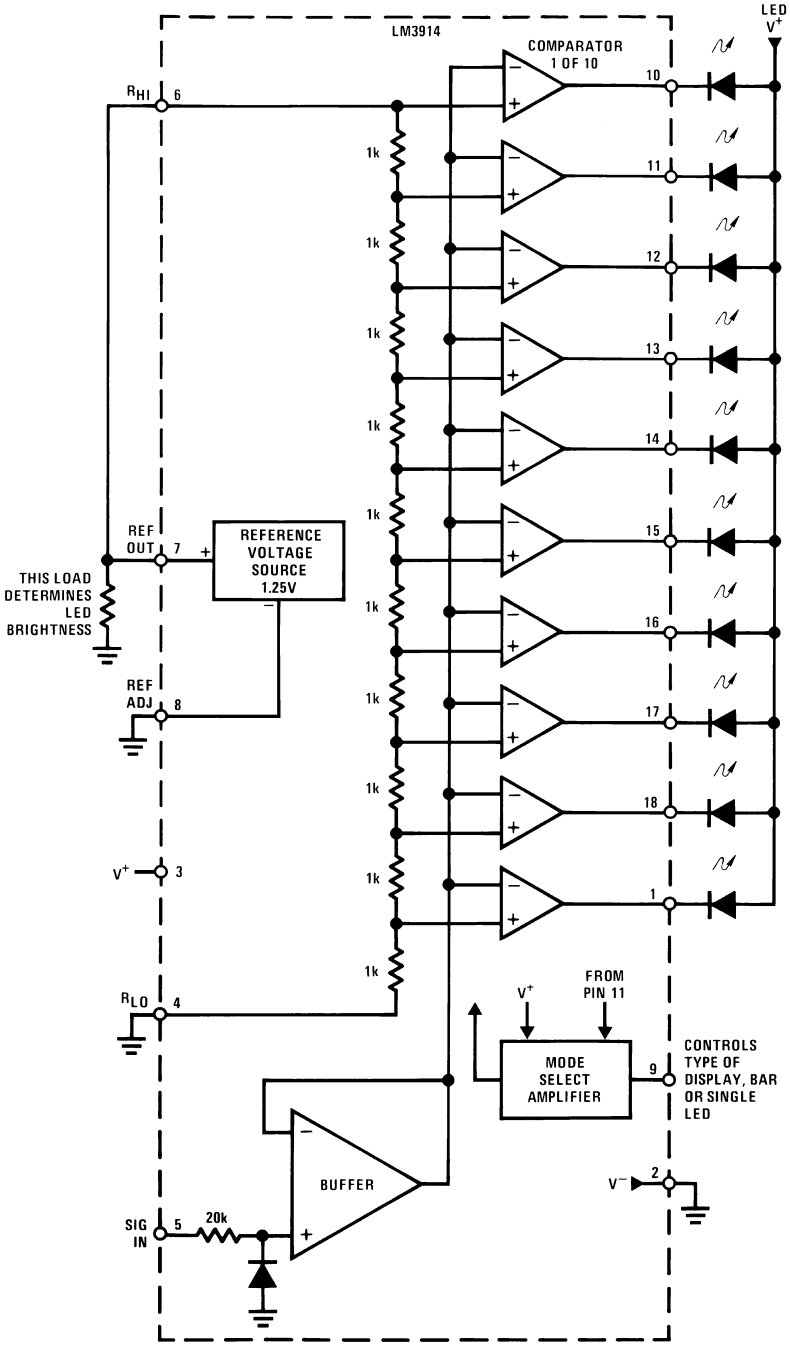
ELECTRICAL CHARACTERISTICS(1)(2)

Parameter	Conditions (1)	Min	Typ	Max	Units
COMPARATOR					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)}$ = 2 mA, I_{LED} = 10 mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE-DIVIDER					
Divider Resistance	Total, Pin 6 to 4	8	12	17	kΩ
Accuracy	(3)		0.5	2	%

(1) Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$
$3\ V_{DC} \le V_{LED} \le V^+$ $0V \le V_{IN} \le V^+ - 1.5V$
$-0.015V \le V_{RLO} \le 12V_{DC}$ T_A = +25°C, $I_{L(REF)}$ = 0.2 mA, V_{LED} = 3.0V, pin 9 connected to pin 3 (Bar Mode).
$-0.015V \le V_{RHI} \le 12\ V_{DC}$For higher power dissipations, pulse testing is used.
(2) Pin 5 input current must be limited to ±3mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.
(3) Accuracy is measured referred to +10.000V_{DC} at pin 6, with 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

BLOCK DIAGRAM

(Showing Simplest Application)



FUNCTIONAL DESCRIPTION

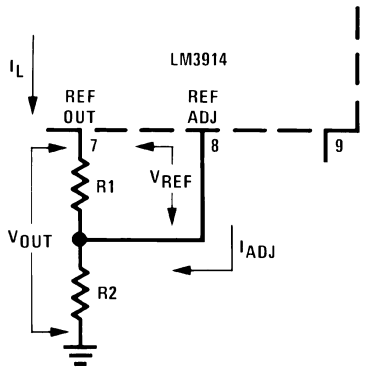
The simplified LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R_2$$



Since the 120µA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

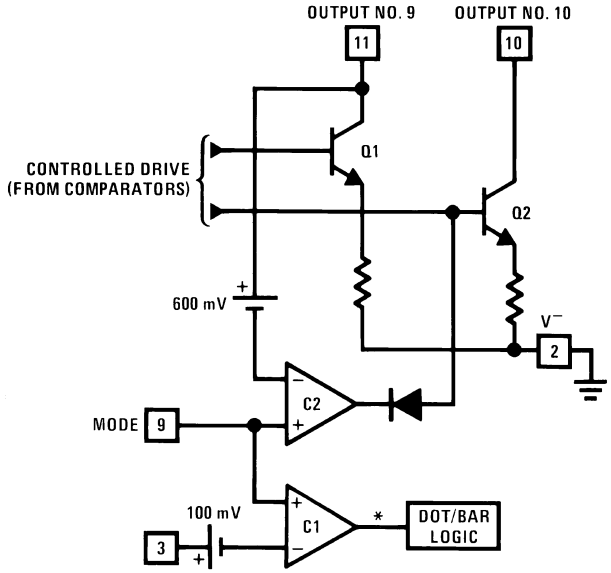
Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

MODE PIN FUNCTIONAL DESCRIPTION

This pin actually performs two functions. Refer to the simplified block diagram below.



*High for bar

Figure 14. Block Diagram of Mode Pin Description

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+ − 100mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100mV reference level, pin 9 should be no more than 20mV below V^+ for bar mode and more than 200mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100µA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100µA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100µA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

FAIRCHILD SEMICONDUCTOR™

September 1983
Revised January 2005

MM74HC132
Quad 2-Input NAND Schmitt Trigger

General Description

The MM74HC132 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC}=4.5V

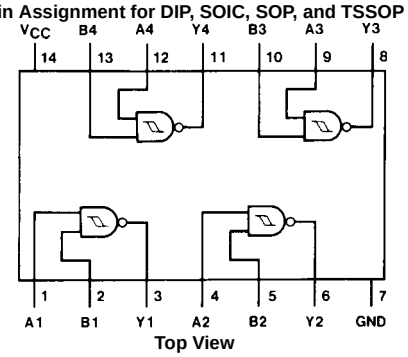
Ordering Code:

Order Number	Package Number	Package Description
MM74HC132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC132MX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC132SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC132N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. (Tape and Reel not available in N14A.)
Pb-Free package per JEDEC J-STD-020B.

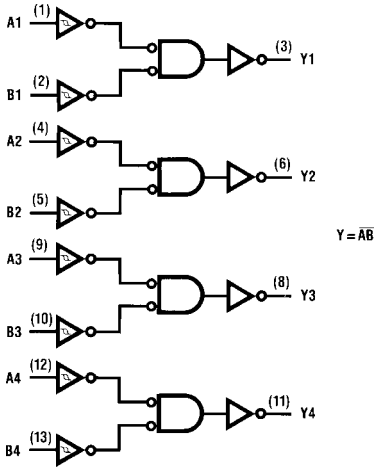
Connection Diagram

Pin Assignment for DIP, SOIC, SOP, and TSSOP



Top View

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+125	°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C	T_A = -40 to 85°C	T_A = -40 to 125°C	Units
					Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage		Min	2.0V		1.0	1.0	1.0	V
				4.5V		2.0	2.0	2.0	V
				6.0V		3.0	3.0	3.0	V
			Max	2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage		Min	2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
			Max	2.0V		1.0	1.0	1.0	V
				4.5V		2.2	2.2	2.2	V
				6.0V		3.0	3.0	3.0	V
V_H	Hysteresis Voltage		Min	2.0V		0.2	0.2	0.2	V
				4.5V		0.4	0.4	0.4	V
				6.0V		0.5	0.5	0.5	V
			Max	2.0V		1.0	1.0	1.0	V
				4.5V		1.4	1.4	1.4	V
				6.0V		1.5	1.5	1.5	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}		2.0V	2.0	1.9	1.9	1.9	V
		$\|I_{OUT}\| \leq 20$ µA		4.5V	4.5	4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL}		6.0V	6.0	5.9	5.9	5.9	V
		$\|I_{OUT}\| \leq 4.0$ mA		4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA		6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}		2.0V	0	0.1	0.1	0.1	V
		$\|I_{OUT}\| \leq 20$ µA		4.5V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}		6.0V	0	0.1	0.1	0.1	V
		$\|I_{OUT}\| \leq 4.0$ mA		4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA		6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND		6.0V		2.0	20	40	µA
		I_{OUT} = 0 µA							

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

FAIRCHILD SEMICONDUCTOR™

September 1983
Revised January 2005

MM74HC74A
Dual D-Type Flip-Flop with Preset and Clear

General Description

The MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

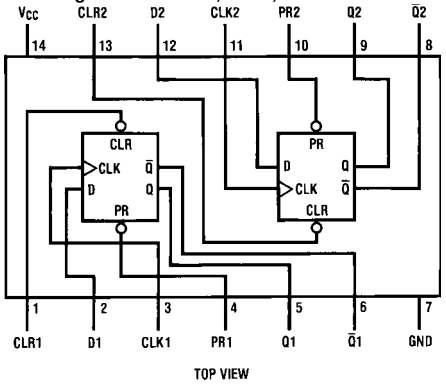
Ordering Code:

Order Number	Package Number	Package Description
MM74HC74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74AMX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74ASJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AMTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



TOP VIEW

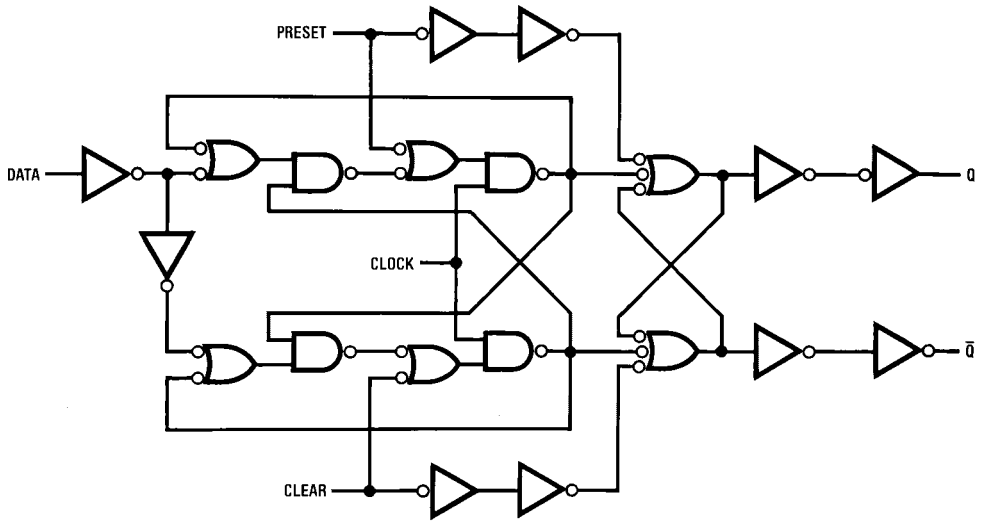
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$ 0

Note: Q0 = the level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Logic Diagram



Absolute Maximum Ratings (Note 2)

(Note 3)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, $_{OUT}$)	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 2: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.3	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0V		4.0	40	80	μA
		I_{OUT} = 0 μA						

Note 5: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

MCP6001/1R/1U/2/4

1 MHz, Low-Power Op Amp

Features

- Available in 5-Lead SC-70 and 5-Lead SOT-23 Packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I_Q = 100 µA (typical)
- Phase Margin: 90° (typical)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

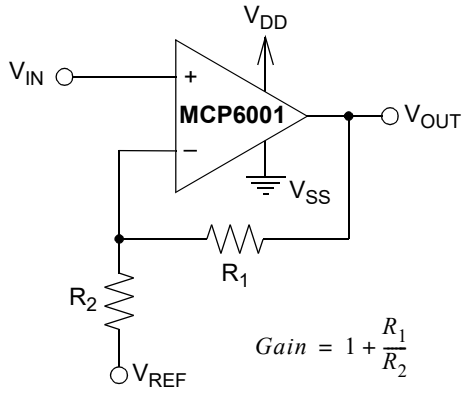
Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer and Analog Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



Noninverting Amplifier

Description

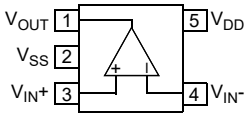
The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains a 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single-supply voltage as low as 1.8V, while drawing 100 µA (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a Common-mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

Package Types

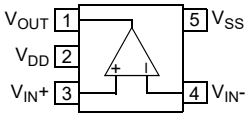
MCP6001

5-Lead SC70, SOT-23



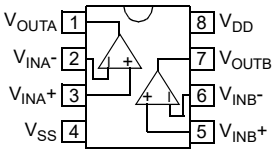
MCP6001R

5-Lead SOT-23



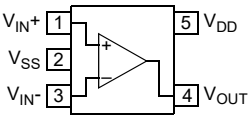
MCP6002

8-Lead PDIP, SOIC, MSOP



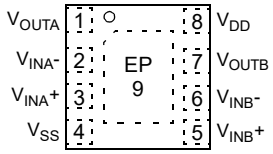
MCP6001U

5-Lead SOT-23



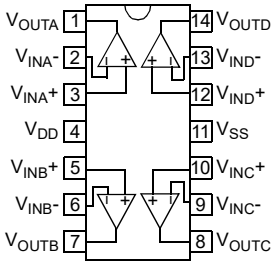
MCP6002

8-Lead 2x3 DFN*



MCP6004

14-Lead PDIP, SOIC, TSSOP



*Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

$V_{DD} - V_{SS}$ 7.0V
Current at Analog Input Pins ($V_{IN}+$, $V_{IN}-$).....±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and $V_{OUT} \approx V_{DD}/2$ (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
Industrial Temperature	I_B	—	19	—	pA	T_A = +85°C
Extended Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common-Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common-Mode						
Common-Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common-Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	**Note 2**
Quiescent Current per Amplifier	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

Note 1: MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

TEXAS INSTRUMENTS

NA555, NE555, SA555, SE555

SLFS022I – SEPTEMBER 1973 – REVISED SEPTEMBER 2014

xx555 Precision Timers

1 Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Fingerprint Biometrics
- Iris Biometrics
- RFID Reader

3 Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

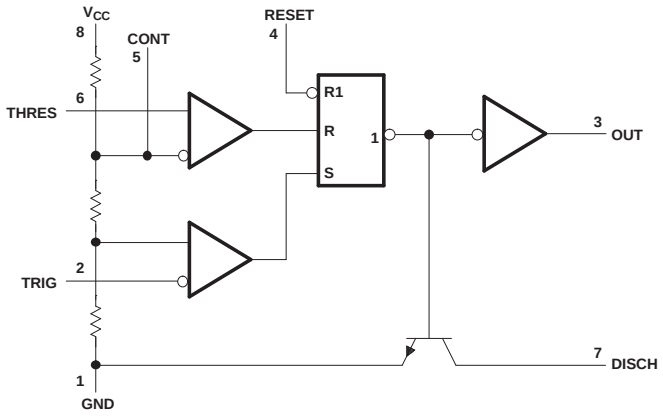
The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
xx555	PDIP (8)	9.81 mm × 6.35 mm
	SOP (8)	6.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

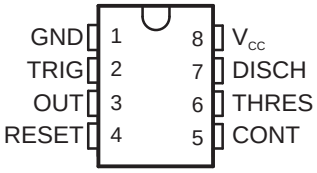
(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

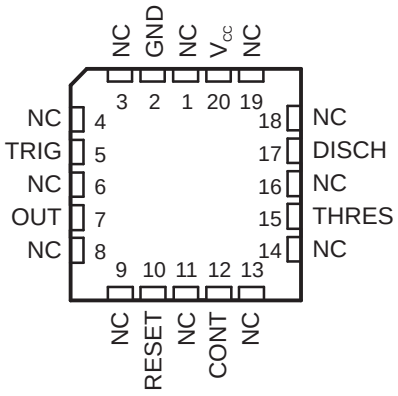


6 Pin Configuration and Functions

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, P, PS, PW, JG	FK		
	NO.			
CONT	5	12	I/O	Controls comparator thresholds, Outputs 2/3 VCC, allows bypass capacitor connection
DISCH	7	17	O	Open collector output to discharge timing capacitor
GND	1	2	–	Ground
NC		1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	–	No internal connection
OUT	3	7	O	High current timer output signal
RESET	4	10	I	Active low reset input forces output and discharge low.
THRES	6	15	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	5	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
V_{CC}	8	20	–	Input supply voltage, 4.5 V to 16 V. (SE555 maximum is 18 V)

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			18	V
V_I	Input voltage	CONT, RESET, THRES, TRIG		V_{CC}	V
I_O	Output current			±225	mA
θ_{JA}	Package thermal impedance(3)(4)	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ_{JC}	Package thermal impedance(5)(6)	FK package		5.61	°C/W
		JG package		14.5	
T_J	Operating virtual junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	JG package		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C) / \theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with MIL-STD-883.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±200	mA
T_A	Operating free-air temperature	NA555	–40	105	°C
		NE555	0	70	
		SA555	–40	85	
		SE555	–55	125	

7.4 Electrical Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current(1)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
		T_A = –55°C to 125°C	3		6				
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
		T_A = –55°C to 125°C			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	µA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T_A = –55°C to 125°C				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			–0.4	–1		–0.4	–1.5	
DISCH switch off-state current				20	100		20	100	nA
DISCH switch on-state voltage	V_{CC} = 5 V, I_O = 8 mA						0.15	0.4	V
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
		T_A = –55°C to 125°C	9.6		10.4				
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
		T_A = –55°C to 125°C	2.9		3.8				
Low-level output voltage	V_{CC} = 15 V, I_{OL} = 10 mA			0.1	0.15		0.1	0.25	V
		T_A = –55°C to 125°C			0.2				
	V_{CC} = 15 V, I_{OL} = 50 mA			0.4	0.5		0.4	0.75	
		T_A = –55°C to 125°C			1				
	V_{CC} = 15 V, I_{OL} = 100 mA			2	2.2		2	2.5	
		T_A = –55°C to 125°C			2.7				
	V_{CC} = 15 V, I_{OL} = 200 mA			2.5			2.5		
	V_{CC} = 5 V, I_{OL} = 3.5 mA	T_A = –55°C to 125°C			0.35				
	V_{CC} = 5 V, I_{OL} = 5 mA			0.1	0.2		0.1	0.35	
		T_A = –55°C to 125°C			0.8				
	V_{CC} = 5 V, I_{OL} = 8 mA			0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V, I_{OH} = –100 mA		13	13.3		12.75	13.3		V
		T_A = –55°C to 125°C	12						
	V_{CC} = 15 V, I_{OH} = –200 mA			12.5			12.5		
	V_{CC} = 5 V, I_{OH} = –100 mA		3	3.3		2.75	3.3		
		T_A = –55°C to 125°C	2						
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

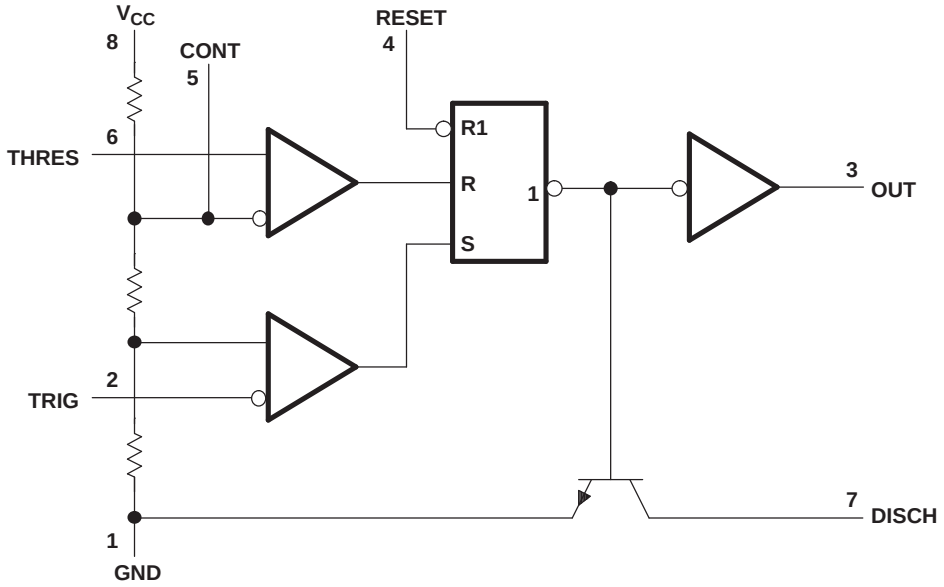
(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is R = R_A + R_B ≠ 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

8 Detailed Description

8.1 Overview

The xx555 timer is a popular and easy to use for general purpose timing applications from 10 µs to hours or from < 1mHz to 100 kHz. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. Maximum output sink and discharge sink current is greater for higher VCC and less for lower VCC.

8.2 Functional Block Diagram



A. Pin numbers shown are for the D, JG, P, PS, and PW packages.

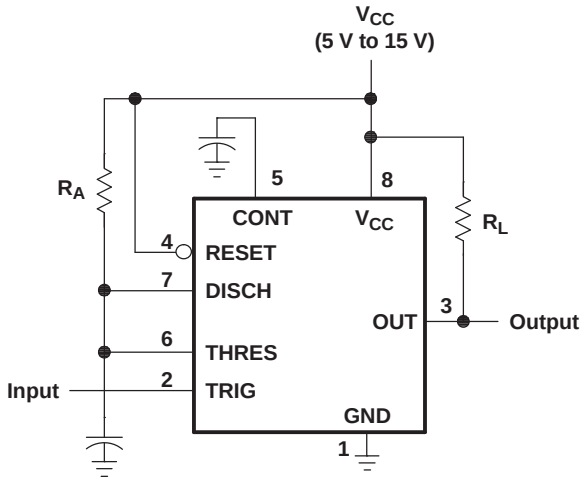
B. RESET can override TRIG, which can override THRES.

8.3 Feature Description

8.3.1 Mono-stable Operation

For mono-stable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 µs, which limits the minimum monostable pulse width to 10 µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

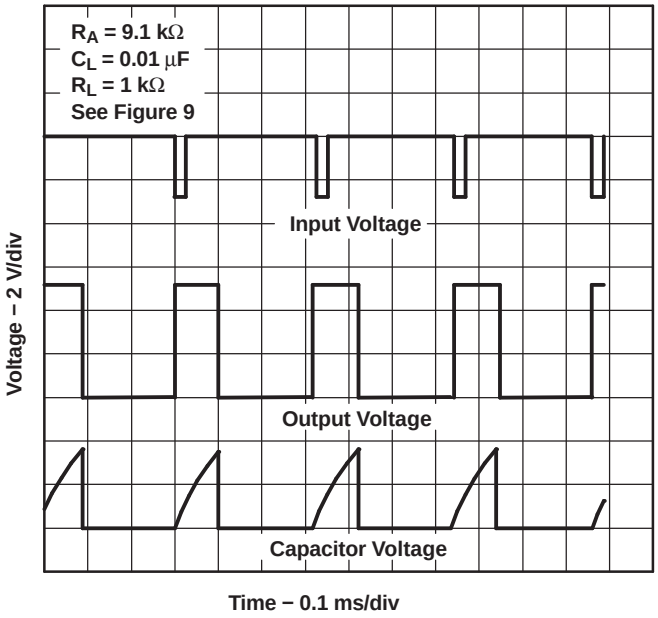


Figure 10. Typical Monostable Waveforms

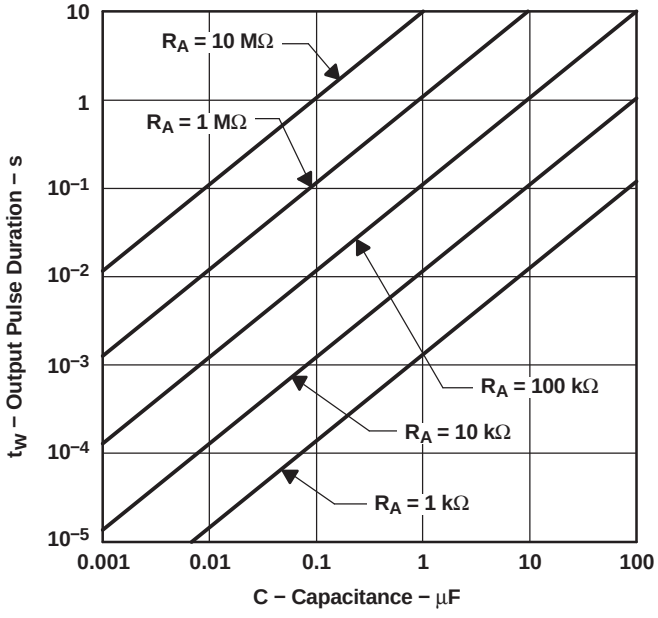


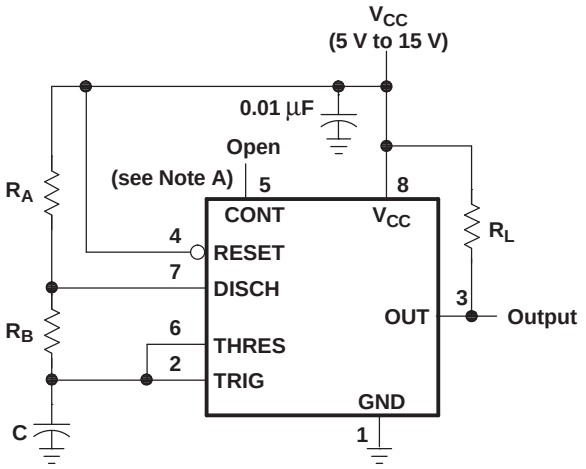
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

8.3.2 A-stable Operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

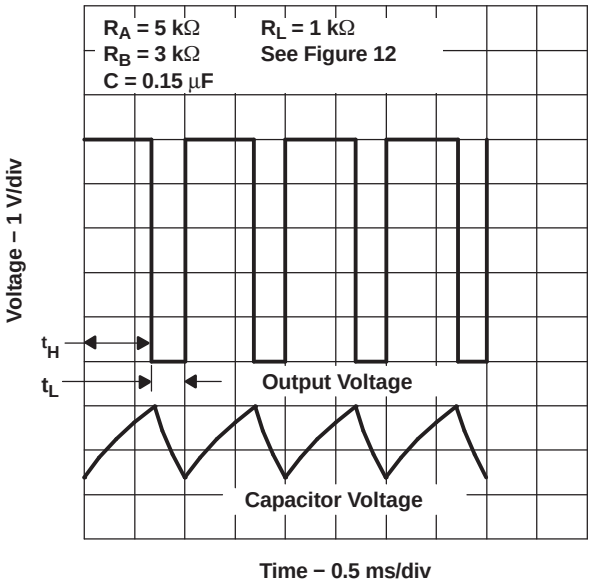


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

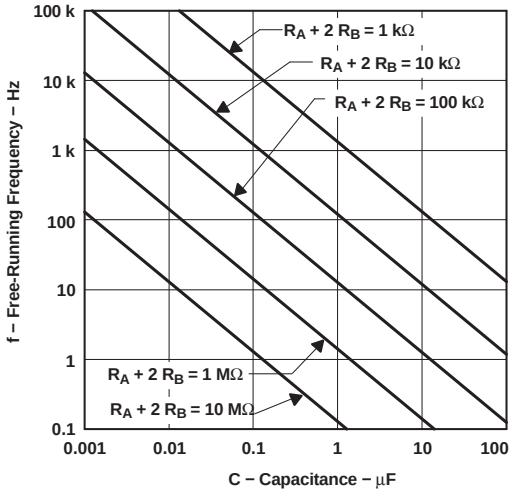


Figure 14. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 15 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

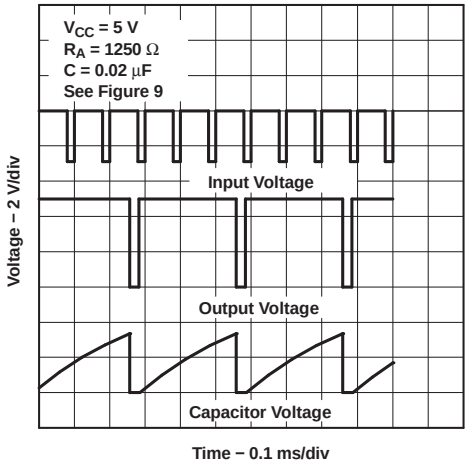


Figure 15. Divide-by-Three Circuit Waveforms

8.4 Device Functional Modes

Table 1. Function Table

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{CC}	Irrelevant	High	Off
High	>1/3 V_{CC}	>2/3 V_{CC}	Low	On
High	>1/3 V_{CC}	<2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

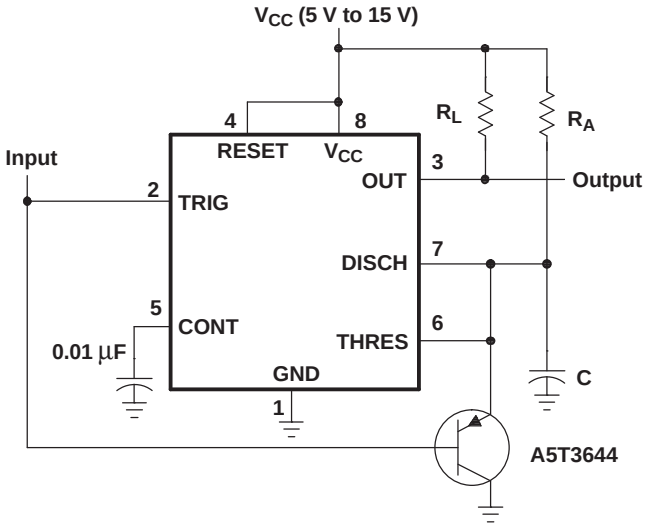
9.1 Application Information

The xx555 timer devices use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in Figure 16 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 17.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 16. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor "C" will remain discharged.

9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C >$ [maximum normal input high time]. R_L improves V_{OH}, but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.1.3 Application Curves

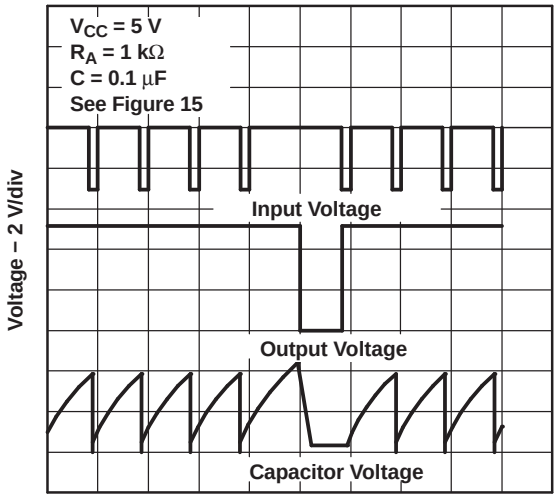
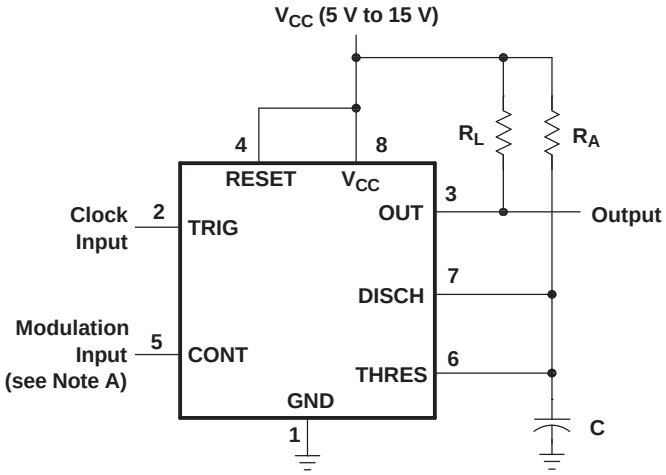


Figure 17. Completed Timing Waveforms for Missing-Pulse Detector

9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

Typical Applications (continued)

9.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 VCC. Modulation input can vary from ground to VCC. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH}, but it is not required for TTL compatibility.

9.2.2.3 Application Curves

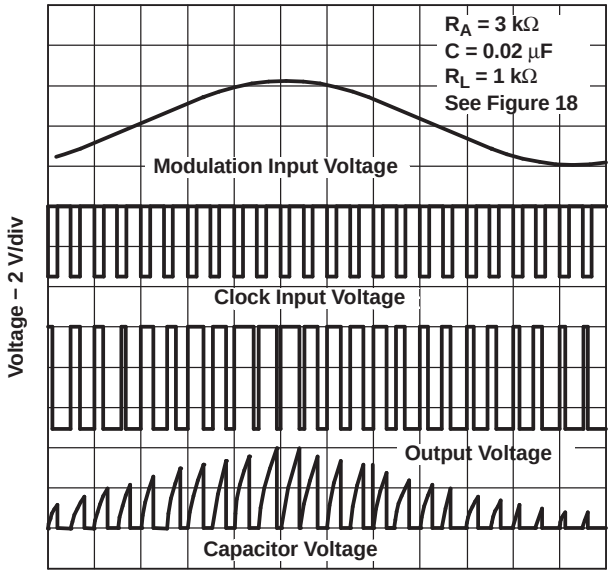
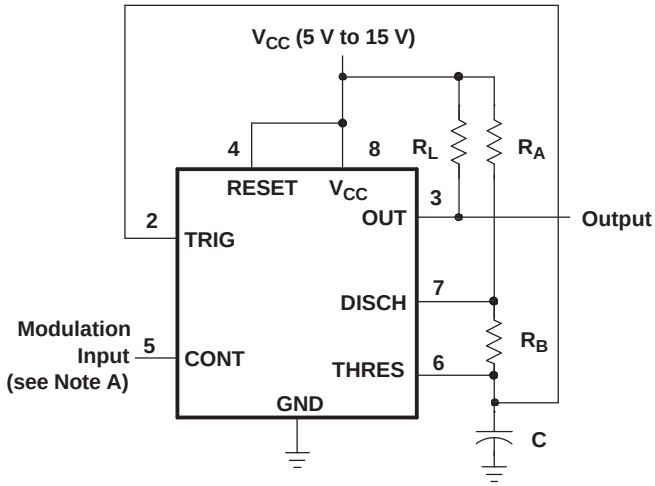


Figure 19. Pulse-Width-Modulation Waveforms

9.2.3 Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

9.2.3.1 Design Requirements

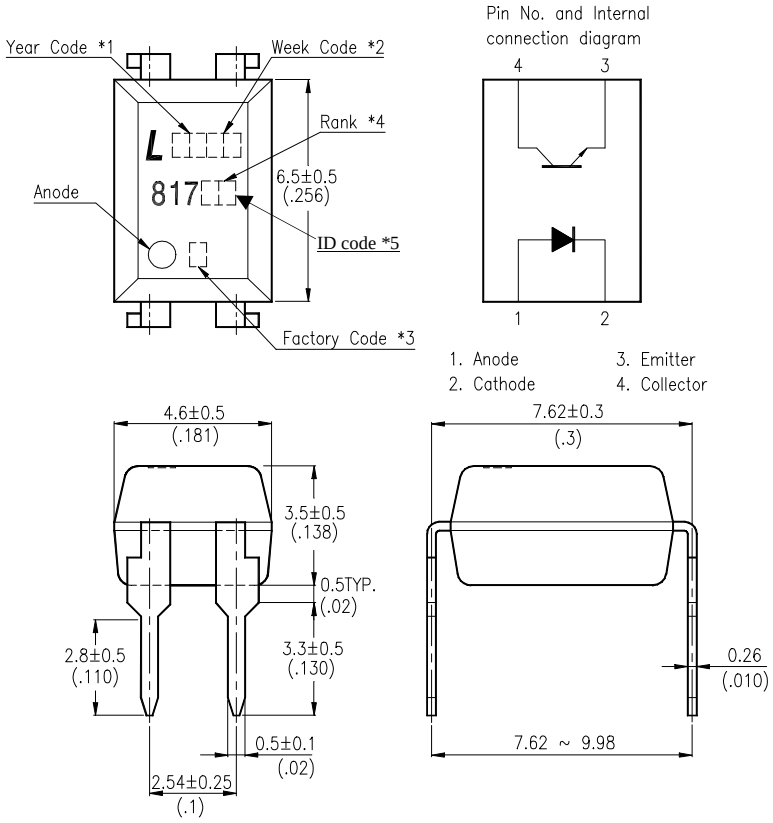
Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in A-stable Operation section. R_L improves V_{OH}, but it is not required for TTL compatibility.

2. PACKAGE DIMENSIONS

2.1 LTV-817-IN



Notes :

1. Year date code.
2. 2-digit work week.
3. Factory identification mark shall be marked
   (Y: Thailand, W: China-CZ, X : China-TJ)
4. Rank shall be or shall not be marked.
5. ID code: —、N、no mark、IN or any indicator character.

* Dimensions are in Millimeters and (Inches).

3. RATING AND CHARACTERISTICS

3.1 Absolute Maximum Ratings at Ta=25°C

	Parameter	Symbol	Rating	Unit
Input	Forward Current	I_F	30	mA
	Reverse Voltage	V_R	5	V
	Power Dissipation	P	49	mW
Output	Collector - Emitter Voltage	V_{CEO}	35	V
	Emitter - Collector Voltage	V_{ECO}	6	V
	Collector Current	I_C	30	mA
	Collector Power Dissipation	P_C	150	mW
	Total Power Dissipation	P_{tot}	150	mW
1.	Isolation Voltage	V_{iso}	5000	V_{rms}
	Operating Temperature	T_{opr}	-55 ~ +110	°C
	Storage Temperature	T_{stg}	-55 ~ +125	°C
2.	Soldering Temperature	T_{sol}	260	°C

1. AC For 1 Minute, R.H. = 40 ~ 60%

   Isolation voltage shall be measured using the following method.

   (1) Short between anode and cathode on the primary side and between collector and emitter on the secondary side.

   (2) The isolation voltage tester with zero-cross circuit shall be used.

   (3) The waveform of applied voltage shall be a sine wave.

2. For 10 Seconds

3.2 ELECTRICAL OPTICAL CHARACTERISTICS at Ta=25°C

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input		Forward Voltage	V_F	—	1.2	1.7	V	I_F=20mA
		Reverse Current	I_R	—	—	20	μA	V_R=4V
		Terminal Capacitance	C_t	—	30	250	pF	V=0, f=1KHz
Output		Collector Dark Current	I_{CEO}	—	—	250	nA	V_{CE}=20V, I_F=0
		Collector-Emitter Breakdown Voltage	BV_{CEO}	35	—	—	V	I_C=0.1mA, I_F=0
		Emitter-Collector Breakdown Voltage	BV_{ECO}	6	—	—	V	I_E=10μA, I_F=0
TRANSFER CHARACTERISTICS		Collector Current	I_C	1.5	—	20	mA	I_F=5mA V_{CE}=5V
	1.	Current Transfer Ratio	CTR	30	—	400	%	
		Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	—	0.1	0.4	V	I_F=20mA I_C=1mA
		Isolation Resistance	R_{iso}	—	5×10^5	—	Ω	DC500V, 40 ~ 60% R.H.
		Floating Capacitance	Cf	—	0.6	1	pF	V=0, f=1MHz
		Response Time (Rise)	tr	—	4	—	μs	V_{CE}=2V, I_C=2mA R_L=100Ω,
		Response Time (Fall)	tf	—	3	—	μs	

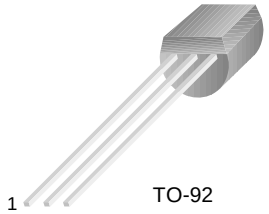
1. $CTR = \frac{I_C}{I_F} \times 100\%$

FAIRCHILD
SEMICONDUCTOR®

BC546/547/548/549/550

Switching and Applications

- High Voltage: BC546, V_{CEO}=65V
- Low Noise: BC549, BC550
- Complement to BC556 ... BC560



TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage : BC546	80	V
	: BC547/550	50	V
	: BC548/549	30	V
V_{CEO}	Collector-Emitter Voltage : BC546	65	V
	: BC547/550	45	V
	: BC548/549	30	V
V_{EBO}	Emitter-Base Voltage : BC546/547	6	V
	: BC548/549/550	5	V
I_C	Collector Current (DC)	100	mA
P_C	Collector Power Dissipation	500	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

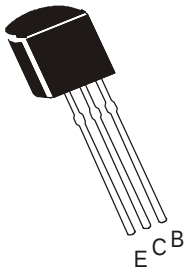
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current	V_{CB}=30V, I_E=0			15	nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=2mA	110		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		90	250	mV
		I_C=100mA, I_B=5mA		200	600	mV
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		700		mV
		I_C=100mA, I_B=5mA		900		mV
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	580	660	700	mV
		V_{CE}=5V, I_C=10mA			720	mV
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=100MHz		300		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Capacitance	V_{EB}=0.5V, I_C=0, f=1MHz		9		pF
NF	Noise Figure : BC546/547/548	V_{CE}=5V, I_C=200μA		2	10	dB
	: BC549/550	f=1KHz, R_G=2KΩ		1.2	4	dB
	: BC549	V_{CE}=5V, I_C=200μA		1.4	4	dB
	: BC550	R_G=2KΩ, f=30~15000MHz		1.4	3	dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

SILICON PLANAR EPITAXIAL TRANSISTORS

BC635, 637, 639 NPN
BC636, 638, 640 PNP



TO-92
Plastic Package
For Lead Free Parts, Device Part # will be Prefixed with "T"

High Current Transistor

ABSOLUTE MAXIMUM RATINGS (T_a=25ºC)

DESCRIPTION	SYMBOL	BC635 / BC636	BC637 / BC638	BC639 / BC640	UNIT
Collector Emitter Voltage	V_{CEO}	45	60	80	V
Collector Base Voltage	V_{CBO}	45	60	80	V
Emitter Base Voltage	V_{EBO}	5.0			V
Collector Current Continuous	I_C	1.0			A
Total Device Dissipation at T_a=25ºC Derate Above 25ºC	P_D	800 6.4			mW mW/ºC
Total Device Dissipation at T_a=25ºC	**P_D	1.0			W
Total Device Dissipation at T_c=25ºC Derate Above 25ºC	P_D	2.75 22			W mW/ºC
Operating And Storage Junction Temperature Range	T_j, T_{stg}	- 55 to +150			ºC

THERMAL RESISTANCE

Junction to Case	$R_{th\ (j-c)}$	45	ºC/W
Junction to Ambient in free air	$R_{th\ (j-a)}$	156	ºC/W
Junction to Ambient	**$R_{th\ (j-a)}$	125	ºC/W

ELECTRICAL CHARACTERISTICS (T_a=25ºC unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Collector Emitter Voltage	V_{CEO}	I_C=1mA, I_B=0			
		BC635/BC636	45		V
		BC637/BC638	60		V
		BC639/BC640	80		V
Collector Base Voltage	V_{CBO}	I_C=100µA, I_E=0			
		BC635/BC636	45		V
		BC637/BC638	60		V
		BC639/BC640	80		V
Emitter Base Voltage	V_{EBO}	I_E=10µA, I_C=0	5.0		V
Collector Cut Off Current	I_{CBO}	V_{CB}=30V, I_E=0		0.1	µA
		V_{CB}=30V, I_E=0, T_a=125ºC		10	µA
Base Emitter (On) Voltage	*$V_{BE\ (on)}$	I_C=500mA, V_{CE}=2V		1.0	V
Collector Emitter Saturation Voltage	*$V_{CE\ (sat)}$	I_C=500mA, I_B=50mA		0.5	V

***Pulse Test: Pulse Width ≤ 300ms, Duty Cycle 2%**

****Transistors mounted on printed circuit board, max Lead Length 4mm, mounting pad for collector lead min 10mm x 10 mm**

BC635_BC640Rev_5 180712E